

# Curriculum Vitae of Juan L. Aragón

(October 2011)

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## ADDRESS

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## SUMMARY

Juan L. Aragón received his M.S. degree in Computer Science in 1996 and his Ph.D. degree in Computer Engineering in 2003, both from the Universidad de Murcia (Spain) followed by a 1-year postdoctoral stay as a Visiting Assistant Professor and Researcher in the Computer Science Department at the University of California, Irvine. In 1999 he joined the Computer Engineering Department at the Universidad de Murcia where he currently is an Associate Professor. His research interests are focused on CMP architectures, core processor microarchitecture, energy-efficient and reliable systems, and gpGPUs.

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## EDUCATION

- Oct'99 – Feb'03      *Ph.D. Degree in Computer Engineering*  
Computer Engineering Department, Universidad de Murcia  
Advisors: José González (UMU) and Antonio González (UPC), both currently at  
*Intel Barcelona Research Center*
- Oct'94 – Jul'96      *M.S. in Computer Engineering*  
Facultad de Informática, Universidad de Murcia
- Oct'91 – Jul'94      *B.S. in Computer Engineering*  
Facultad de Informática, Universidad de Murcia
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## EXPERIENCE

- Oct'07 – *present*      *Associate Professor*  
Computer Engineering Department, Universidad de Murcia (Spain)
- Undergraduate Courses:
- Computer Architecture (2007-2011)
  - Advanced Computer Architecture (2011)
  - Introduction to Computer Organization (2007-2009)
  - Operating Systems (2009)
- Master Courses:
- Advanced Aspects on General Purpose Multicore Architectures (2010-2011)
  - Technologies and Architectures for Embedded Systems (2007-2010)
- May'06 – Sep'08      *Vice Dean for Student Affairs*  
School of Computer Science, Universidad de Murcia (Spain)

- Oct'99 – Oct'07      *Assistant Professor*  
 Computer Engineering Department, Universidad de Murcia (Spain)
- Undergraduate Courses:
- Introduction to Computer Organization (1999-2007)
  - Logic Design and Digital Systems (1999-2003)
  - Computer Architecture (2004-2007)
- Master Courses:
- Grid Computing (year 2004)
  - High Performance Architectures for Embedded Systems (2005)
  - Technologies and Architectures for Embedded Systems (2006-2007)
- Jun'03 – June'04      *Visiting Assistant Professor and Researcher*  
 Computer Science Dept., University of California, Irvine (CA, USA)
- Undergraduate Courses:
- ICS-152: Computer Systems Architecture (Fall-2003 and Winter-2004)
- Sep'97 – Sep'99      *Graduate Researcher*  
 Physics Department, Universidad de Murcia (Spain)  
 I was involved in several research projects in the Optics Research Group, developing several real-time systems to analyze and process digital images from the human retina.
- Mar 1, 99 – Apr 30, 99      Internship at the Center for Visual Science, University of Rochester (NY, USA)  
 Developing a real-time digital image processing application to determine the ocular wave aberration of the human eye.
- May'97 – Sep'97      *Systems Manager*  
 Computer Science Department, Universidad de Murcia (Spain)  
 Managing a cluster of Sun UltraSparc-I workstations and working in parallel algorithms using High Performance Fortran (HPF).

## FELLOWSHIPS & GRANTS RECEIVED

- Sep'10 – Dec'10      HiPEAC Collaboration Grant: “Effects of a temperature-aware scheduler in a 3D-stacked architecture”, in collaboration with Prof. Stefanos Kaxiras (University of Uppsala). Granted by HiPEAC-2 European Network of Excellence (5000€)
- Sep'10 – Dec'10      HiPEAC Collaboration Grant: “The Implications of Near Threshold Last Level Cache Operation for Parallel Workloads”, in collaboration with Prof. Yiannakis Sazeides (Univ. Cyprus). Granted by HiPEAC-2 EU Network of Excellence (5000€)
- Dec'07 – May'08      HiPEAC Research Cluster #1173: “Efficient microarchitectural policies under power constraints at minimal performance cost”, in collaboration with Prof. Stefanos Kaxiras. Granted by HiPEAC European Network of Excellence (7500€)
- May'05 – July'05      HiPEAC Research Cluster #355: “Energy-efficient single-core processor design”, in collaboration with Prof. Stefanos Kaxiras (University of Patras, Greece)  
 Granted by HiPEAC European Network of Excellence (4000€)

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| Dec'03 – June'04 | Post-doctoral Fellowship (Beca de Formación Post-doctoral)<br>Granted by Fundación Séneca, Región de Murcia (Spain)   |
| Sep'97 – Sep'99  | Pre-doctoral Fellowship (Beca FPI de Formación Pre-doctoral)<br>Granted by Fundación Séneca, Región de Murcia (Spain) |

## PUBLICATIONS

### JOURNALS:

- [J.1] D. Sánchez, J.L. Aragón and J.M. García. “A Fault-Tolerant Architecture for Parallel Applications in Tiled-CMPs”. *To appear in The Journal of Supercomputing*, [doi: 10.1007/s11227-011-0670-9]
- [J.2] J.M. Cebrián, J.L. Aragón, J.M. García and S. Kaxiras. “Leakage-efficient Design of Value Predictors through State and Non-state Preserving Techniques”. *The Journal of Supercomputing*, vol. 55, no. 1, pp. 28-50, ISSN: 0920-8542, January 2011
- [J.3] A. Flores, M.E. Acacio and J.L. Aragón. “Exploiting Address Compression and Heterogeneous Interconnects for Efficient Message Management in Tiled CMPs”. *Journal of Systems Architecture*, vol. 56, no. 9, pp. 429-441, ISSN: 1383-7621, September 2010
- [J.4] A. Flores, J.L. Aragón and M.E. Acacio. “Heterogeneous Interconnects for Energy-Efficient Message Management in CMPs”. *IEEE Transactions on Computers*, vol. 59, no. 1, pp. 16-28, ISSN: 0018-9340, January 2010
- [J.5] J.L. Aragón and A. Veidenbaum. “Optimizing CAM-Based Instruction Cache Designs for Low-Power Embedded Systems”. *Journal of Systems Architecture*, vol. 54, no. 12, pp. 1155-1163, ISSN: 1383-7621, December 2008
- [J.6] A. Flores, J.L. Aragón and M.E. Acacio. “An Energy Consumption Characterization of On-Chip Interconnection Networks for Tiled CMP Architectures”. *The Journal of Supercomputing*, vol. 45, no. 3, pp. 341-364, ISSN: 0920-8542, September 2008
- [J.7] J.L. Aragón, J. González and A. González. “Control Speculation for Energy-Efficient Next-Generation Superscalar Processors”. *IEEE Transactions on Computers*, vol. 55, no. 3, pp. 281-291, ISSN: 0018-9340, March 2006
- [J.8] J.L. Aragón, J. González and A. González. “Reducing Branch Misprediction Penalty through Confidence Estimation”. *Journal of Computer Science & Technology*, vol. 3, no. 1, ISSN: 1666-6038, April 2003
- [J.9] J.M. Cebrián, J.L. Aragón and S. Kaxiras. “Inter-core Balancing for Efficient Power and Thermal Management in CMPs”. *Submitted for review*
- [J.10] D. Sánchez, J.L. Aragón and J.M. García. “Soft-Error Mitigation by means of Decoupled Transactional Memory Threads”. *Submitted for review*
- [J.11] J.M. Cebrián, J.L. Aragón and S. Kaxiras. “Managing Power Constraints in a Single-core Scenario through Power Tokens”. *Submitted for review*

### CONFERENCES:

- [C.1] J.M. Cebrián, J.L. Aragón and S. Kaxiras. “Token3D: Reducing Temperature in 3D die-stacked CMPs through Cycle-level Power Control Mechanisms”. *Proc. of the 17th Int. Conference on Parallel and Distributed Computing (Euro-Par)*, Bordeaux, France, pp. 295-309, ISBN: 978-3-

- 642-23399-9. *Lecture Notes in Computer Science*, vol. 6852, Springer-Verlag, pp. 295-309, ISSN: 0302-9743, August 2011
- [C.2] D. Sánchez, Y. Sazeides, J.L. Aragón and J.M. García. “An Analytical Model for the Calculation of the Expected Miss Ratio in Faulty Caches”. *Proc. of the 17th IEEE International On-Line Testing Symposium (IOLTS)*, Athens, Greece, pp. 287-292, ISBN: 978-1-4577-1054-4, July 2011
- [C.3] J.M. Cebrián, J.L. Aragón and S. Kaxiras. “Power Token Balancing: Adapting CMPs to Power Constraints for Parallel Multithreaded Workloads”. *Proc. of the 25th IEEE Int. Parallel and Distributed Processing Symposium (IPDPS)*, Anchorage, Alaska, USA, pp. 431-442, ISBN: 978-0-7695-4385-7, May 2011
- [C.4] D. Sánchez, J.L. Aragón and J.M. García. “A Log-Based Redundant Architecture for Reliable Parallel Computation”. *Proc. of the 17th Int. Conference on High Performance Computing (HiPC)*, Goa, India, pp. 1-10, ISBN: 978-1-4244-8519-2, December 2010
- [C.5] P. Petoumenos, G. Psychou, S. Kaxiras, J.M. Cebrián and J.L. Aragón. “MLP-aware Instruction Queue Resizing: The Key to Power-Efficient Performance”. *Proc. of the 23rd Int. Conference on Architecture of Computing Systems (ARCS)*, Hannover, Germany, pp. 113-125, ISBN: 3-642-11949-2. *Lecture Notes in Computer Science*, vol. 5974, Springer-Verlag, pp. 113-125, ISSN: 0302-9743, February 2010
- [C.6] A. Flores, J.L. Aragón and M.E. Acacio. “Energy-Efficient Hardware Prefetching for CMPs using Heterogeneous Interconnects”. *Proc. of the 18th Euromicro International Conference on Parallel, Distributed and Network-Based Computing (EUROMICRO-PDP)*, Pisa, Italy, pp. 147-154, ISBN: 0-7695-3939-3, February 2010
- [C.7] K.E. Østby, J.L. Aragón, J.M. García and M. Ujaldón. “FATSEA – An Architectural Simulator for General Purpose Computing on GPUs”. *Proc. of the 2nd Workshop on Rapid Simulation & Performance Evaluation: Methods and Tools (RAPIDO)*, in conjunction with HiPEAC'10, Pisa, Italy, pp. 1-6, ISBN: 3-642-11514-4, January 2010
- [C.8] D. Sánchez, J.L. Aragón and J.M. García. “REPAS: Reliable Execution for Parallel Applications in Tiled-CMPs”. *Proc. of the 15th Int. Conference on Parallel and Distributed Computing (Euro-Par)*, Delft, Netherlands, pp. 321-333, ISBN: 978-3-642-03868-6. *Lecture Notes in Computer Science*, vol. 5704, Springer-Verlag, pp. 321-333, ISSN: 0302-9743, August 2009
- [C.9] J.M. Cebrián, J.L. Aragón, J.M. García, P. Petoumenos and S. Kaxiras. “Efficient Microarchitecture Policies for Accurately Adapting to Power Constraints”. *Proc. of the 23rd IEEE Int. Parallel and Distributed Processing Symposium (IPDPS)*, Rome, Italy, pp. 1-12, ISBN: 978-1-4244-3750-4, May 2009
- [C.10] D. Sánchez, J.L. Aragón and J.M. García. “Extending SRT for Parallel Applications in Tiled-CMP Architectures”. *Proc. of the 14th IEEE Workshop on Dependable Parallel, Distributed and Network-Centric Systems (DPDNS)*, in conjunction with IPDPS'09, Rome, Italy, pp. 1-10, ISBN: 978-1-4244-3750-4, May 2009
- [C.11] A. Flores, M.E. Acacio and J.L. Aragón. “Address Compression and Heterogeneous Interconnects for Energy-Efficient High-Performance in Tiled CMPs”. *Proc. of the 37th IEEE Int. Conference on Parallel Processing (ICPP)*, Portland, OR, USA, pp. 295-303, ISBN: 978-0-7695-3374-2, Sep. 2008
- [C.12] D. Sánchez, J.L. Aragón and J.M. García. “Evaluating Dynamic Core Coupling in a Scalable Tiled-CMP Architecture”. *Proc. of the 7th Int. Workshop on Duplicating, Deconstructing, and Debunking (WDDD)*, in conjunction with ISCA'08, Beijing, China, pp. 1-10, ISBN: 978-0-7695-3174-8, June 2008

- [C.13] A. Flores, J.L. Aragón and M.E. Acacio. “Efficient Message Management in Tiled CMP Architectures using a Heterogeneous Interconnection Network”. *Proc. of the 14th Int. Conference on High Performance Computing (HiPC)*, Goa, India, ISBN: 3-540-77219-7. *Lecture Notes in Computer Science*, vol. 4873, Springer-Verlag, pp. 133-146, ISSN: 0302-9743, Dec. 2007
- [C.14] J.M. Cebrián, J.L. Aragón, J.M. García and S. Kaxiras. “Adaptive VP Decay: Making Value Predictors Leakage-efficient Designs for High Performance Processors”. *Proc. of the 4th ACM Int. Conference on Computing Frontiers (CF)*, Ischia, Italy, pp. 113-122, ISBN: 978-1-59593-683-7, May 2007
- [C.15] A. Flores, J.L. Aragón and M.E. Acacio. “Sim-PowerCMP: A Detailed Simulator for Energy Consumption Analysis in Future Embedded CMP Architectures”. *Proc. of the 4th IEEE Int. Symp. on Embedded Computing (SEC)*, Niagara Falls, Canada, pp. 752-757, ISBN: 0-7695-2847-3, May 2007
- [C.16] J.M. Cebrián, J.L. Aragón and J.M. García. “Leakage Energy Reduction in Value Predictors through Static Decay”. *Proc. of the Int. Workshop on High-Performance, Power-Aware Computing (HP-PAC), in conjunction with IPDPS’2007*, Long Beach, CA (USA), pp. 269-275, ISBN: 1-4244-0909-8, March 2007
- [C.17] J.L. Aragón and A. Veidenbaum. “Energy-Effective Instruction Fetch Unit for Wide Issue Processors”. *Proc. of the 10th Asia-Pacific Computer Systems Architecture Conference (ACSAC)*, Singapore, ISBN: 3-540-29643-3. *Lecture Notes in Computer Science*, vol. 3740, Springer-Verlag, pp. 15-27, ISSN: 0302-9743, October 2005
- [C.18] J.L. Aragón, D. Nicolaescu, A. Veidenbaum and A.M. Badulescu. “Energy-Efficient Design for Highly Associative Instruction Caches in Next-Generation Embedded Processors”. *Proc. of the IEEE Int. Conference on Design, Automation and Test in Europe (DATE)*, Paris, France, pp. 1374-1375, ISBN: 0-7695-2085-5, Feb. 2004
- [C.19] J.L. Aragón, J. González and A. González. “Power-Aware Control Speculation through Selective Throttling”. *Proc. of the 9th IEEE Int. Symposium on High Performance Computer Architecture (HPCA)*, Anaheim, CA (USA), pp. 103-112, ISBN: 0-7695-1871-0, Feb. 2003
- [C.20] J.L. Aragón, J. González, A. González and J.E. Smith. “Dual Path Instruction Processing”. *Proc. of the 16th ACM Int. Conference on Supercomputing (ICS)*, New York, NY (USA), pp. 220-229, ISBN: 1-58113-483-5, June 2002
- [C.21] J.L. Aragón, J. González, J.M. García and A. González. “Confidence Estimation for Branch Prediction Reversal”. *Proc. of the 8th Int. Conference on High Performance Computing (HiPC)*, Hyderabad (India), ISBN: 3-540-43009-1. *Lecture Notes in Computer Science*, vol. 2228, Springer-Verlag, pp. 214-223, ISSN: 0302-9743, Dec. 2001
- [C.22] J.L. Aragón, J. González, J.M. García and A. González. “Selective Branch Prediction Reversal by Correlating with Data Values and Control Flow”. *Proc. of the 19th IEEE Int. Conference on Computer Design (ICCD)*, Austin, TX (USA), pp. 228-233, ISBN: 0-7695-1200-3, Sep. 2001

#### NATIONAL (SPANISH) CONFERENCES:

- [C.23] A. Flores, M.E. Acacio and J.L. Aragón. “Reducing the Energy Consumption of Hardware Prefetching in Many-Core CMPs using Reply Partitioning”. *Proc. of the XXII Jornadas de Paralelismo*, pp. 227-232, ISBN: 978-84-694-1791-1, La Laguna (Spain), September 2011
- [C.24] D. Sánchez, Y. Sazeides, J.L. Aragón and J.M. García. “Modelling Permanent Fault Impact on Cache Performance”. *Proc. of the XXII Jornadas de Paralelismo*, pp. 233-238, ISBN: 978-84-694-1791-1, La Laguna (Spain), September 2011

- [C.25] J.M. Cebrián, J.L. Aragón and S. Kaxiras. “Mechanisms to Match Power Constraints in CMPs”. *Proc. of the XXI Jornadas de Paralelismo*, pp. 185-192, ISBN: 978-84-92812-49-3, Valencia (Spain), September 2010
- [C.26] A. Flores, J.L. Aragón and M.E. Acacio. “Hardware Prefetching in Heterogeneous Interconnects: an Approach to Reducing Energy Consumption in Many-Core CMPs”. *Proc. of the XXI Jornadas de Paralelismo*, pp. 177-184, ISBN: 978-84-92812-49-3, Valencia (Spain), September 2010
- [C.27] J.M. Cebrián, J.L. Aragón, J.M. García, P. Petoumenos and S. Kaxiras. “Energy-Efficient Power Budget Matching”. *Proc. of the XX Jornadas de Paralelismo*, pp. 195-200, ISBN: 84-9749-346-8, A Coruña (Spain), Septiembre 2009
- [C.28] A. Flores, M.E. Acacio and J.L. Aragón. “Power-Aware On-Chip Network Management in Tiled CMPs using Address Compression”. *Proc. of the XIX Jornadas de Paralelismo*, pp. 205-210, ISBN: 978-84-8021-676-0, Castellón (Spain), September 2008
- [C.29] D. Sánchez, J.L. Aragón and J.M. García. “Adapting Dynamic Core Coupling to a Direct-Network Environment”. *Proc. of the XIX Jornadas de Paralelismo*, pp. 253-258, ISBN: 978-84-8021-676-0, Castellón (Spain), September 2008
- [C.30] J.M. Cebrián, J.L. Aragón, J.M. García and S. Kaxiras. “An Adaptive Approach for Reducing Leakage Energy Consumption in Value Predictors”. *Proc. of the XVIII Jornadas de Paralelismo*, pp. 107-114, ISBN: 978-84-9732-593-6, Zaragoza (Spain), September 2007
- [C.31] J.M. Cebrián, J.L. Aragón and J.M. García. “Reducing Leakage in Value Predictors by Using Decay Techniques”. *Proc. of the XVII Jornadas de Paralelismo*, pp. 61-66, ISBN: 84-690-0551-0, Albacete (Spain), September 2006
- [C.32] A. Flores, J.L. Aragón and M.E. Acacio. “Sim-PowerCMP: Un simulador de consumo para CMPs”. *Proc. of the XVII Jornadas de Paralelismo*, pp. 85-90, ISBN: 84-690-0551-0, Albacete (Spain), September 2006
- [C.33] J.L. Aragón and A. Veidenbaum. “Low-power Fetch Unit Design for Superscalar Processors”. *Proc. of the XV Jornadas de Paralelismo*, pp. 173-178, ISBN: 84-8240-714-7, Almería (Spain), September 2004
- [C.34] J.L. Aragón, J. González, J.M. García and A. González. “Branch Prediction Reversal by Correlating with Data Values”. *Proc. of the XII Jornadas de Paralelismo (XII Spanish Workshop on Parallelism)*, pp. 9-14, ISBN: 84-9705-043-6, Valencia (Spain), September 2001

#### PHYSICS JOURNALS & CONFERENCES:

- [P.1] H. Hofer, P. Artal, J.L. Aragón and D.R. Williams. “Dynamics of the eye’s wave aberration”. *Journal of the Optical Society of America A*, 18(3), pp. 497-506, ISSN: 0740-3232, March 2001
- [P.2] J.L. Aragón, N. López-Gil and P. Artal. “Real-time double-pass system to study the dynamics of the eye's optical performance”. *Proc. of the EOS Topical Meeting on Physiological Optics*, pp. 49-50, ISSN:1167-5357, Wroclaw (Poland), Sep. 1999
- [P.3] P. Artal, H.J. Hofer, D.R. Williams and J.L. Aragón. “Dynamics of ocular aberrations during accommodation”. *Proc. of the OSA Annual Meeting*, California (USA), Sep. 1999
- [P.4] P. Artal, J.L. Aragón, P.M. Prieto, F. Vargas-Martín and E. Berrio. “Hartmann-Shack wavefront sensor in the eye: accuracy and performance limits”. *Proc. of the Int. Workshop on Adaptive Optics for Industry and Medicine*, pp. 39-44, ISBN: 981-02-4115-1, Durham (England), July 1999
- [P.5] H.J. Hofer, P. Artal, J.L. Aragón and D.R. Williams. “Temporal characteristics of the eye's aberrations”. *Journal of Inv. Ophth. Vis.Sci.*, Sppl. 40, 4, ISSN: 0146-0404, May 1999

## PATENTS:

- *Title:* “Rapid, Automatic measurement of the eye's wave aberration”  
*Inventors:* D.R. Williams, W.J. Vaughn, B.D. Singer, H. Hofer, G.Y. Yoon, P. Artal, J.L. Aragón, P. Prieto and F. Vargas.
  1. US Patent No.: 6,199,986 B1 (Mar. 13th, 2001)
  2. US Patent No.: 6,827,444 B2 (Dec. 7th, 2004)
  3. Singapore Patent No.: P-88309 (June 30th, 2005)
  4. Japan Patent No.: 4660047 (Jan. 7th, 2011)

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## **RESEARCH PROJECTS PARTICIPATION**

1. *Project:* “Arquitecturas de Servidores, Aplicaciones y Servicios”  
*Main Coordinator:* José Duato, UPV, Spain  
*Granted by:* Spanish MEC, TIN2009-14475-C04-02, years 2010-2012
2. *Project:* “Arquitecturas Fiables y de Altas Prestaciones para Centros de Proceso de Datos y Servidores de Internet”  
*Main Coordinator:* José Duato, UPV, Spain  
*Granted by:* Spanish MEC – Prog. Consolider-Ingenio 2010, CSD2006-00046, years 2006-2011
3. *Project:* “Diseño de Arquitecturas CMP Eficientes Energéticamente y Fiables para Sistemas Empotrados de Próxima Generación”  
*Main Coordinator:* José Manuel García Carrasco, UMU, Spain  
*Granted by:* Fundación Séneca, Región de Murcia, 05831/PI/07, years 2007-2009
4. *Project:* “Mejora de las prestaciones, servicios y aplicaciones ofrecidas por arquitecturas cluster de altas prestaciones”  
*Main Coordinator:* José Duato, UPV, Spain  
*Granted by:* Spanish MEC, TIN2006-15516-C04-03, years 2006-2007
5. *Network of Excellence:* “High Performance Embedded Architectures and Compilers (HiPEAC)”.  
*Main Coordinator:* Mateo Valero, UPC, Spain  
*Granted by:* European Union, years 2004-2009
6. *Project:* “Mejora de las prestaciones y servicios ofrecidos por los clusters de computadores personales. Desarrollo de aplicaciones multimedia distribuidas II”  
*Main Coordinator:* José Duato, UPV, Spain  
*Granted by:* Spanish CICYT, TIC2003-08154-C06-03, years 2003-2006
7. *Project:* “Mejora de las prestaciones y servicios ofrecidos por las redes de computadores personales. Desarrollo de aplicaciones multimedia distribuidas”  
*Main Coordinator:* José Duato, UPV, Spain  
*Granted by:* Spanish CICYT, TIC2000-1151-C07-03, years 2001-2003
8. *Project:* “Desarrollo de una red de estaciones de trabajo de altas prestaciones y bajo coste”  
*Main Coordinator:* José Duato, UPV, Spain  
*Granted by:* Spanish CICYT, TIC97-0897-C04-03, years 1997-2000
9. *Project:* “Estudios fundamentales en óptica fisiológica: óptica adaptativa, polarización, acomodación y modelización”  
*Main Coordinator:* Pablo Artal, UMU, Spain  
*Granted by:* Spanish CICYT, PB97-1056, years 1998-2000.

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## Ph.D. STUDENTS

1. Antonio Flores. “Improving the Performance and Reducing the Consumption of Multicore Processors using Heterogeneous Networks”  
*Advisors:* Juan L. Aragón and Manuel E. Acacio  
*Graduated on:* September 24th, 2010  
*Qualification:* Summa cum laude
2. Daniel Sánchez. “Microarchitectural Approaches for Hardware Fault Mitigation in Multicore Processors”  
*Advisors:* Juan L. Aragón and José M. García  
*Graduated on:* July 25th, 2011  
*Qualification:* Summa cum laude
3. Juan M. Cebrián. “Efficient Power and Thermal Management using Fine-grain Architectural Approaches in Multicores”  
*Advisors:* Juan L. Aragón and Stefanos Kaxiras  
*Graduated on:* September 5th, 2011  
*Qualification:* Summa cum laude

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## OTHER ACTIVITIES

- Program Committee member: EUROMICRO-PDP-2009, EUROMICRO-PDP-2010, EUROMICRO-PDP-2011, EUROMICRO-PDP-2012, ISLPED-2010
- Conference reviewer for: ISCA-2001, PDP-2002, ICCD-2002, HPCA-2003, ISCA-2003, ICS-2003, IWIA-2003, ESTImedia-2003, HPCA-2004, ACSAC-2004, PACT-2004, ICCD-2004, MICRO-2004, ICPP-2005, HiPC-2005, ISCA-2006, CASES-2007, EUROMICRO-PDP-2009, IPDPS-2009, Hot Interconnects-2009, HPCA-2010, EUROMICRO-PDP-2010, ISLPED-2010, EUROMICRO-PDP-2011, HPCA-2011, EUROMICRO-PDP-2012
- Journal reviewer for: IEEE Transactions on Computers (2002, 2005, 2006, 2007), IEE Computers and Digital Techniques Journal (2003, 2004), Journal of Systems Architecture (2003), Journal of Computer Science and Technology (2006), LNCS Transactions on HiPEAC (2007), IEEE Computer (2007, 2009), EURASIP Journal on Embedded Systems (2007), IEEE Transactions on Very Large Scale Integration Systems (2009), IEEE Computer Architecture Letters (2010)
- IEEE Computer Society Member