

Manuel E. Acacio

- RESUME -
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ADDRESS

Departamento de Ingeniería y Tecnología de Computadores
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RESEARCH INTERESTS

Broad Category: Computer Architecture, Multiprocessor Architecture

Specific Areas Include: Chip-multiprocessor architectures (CMPs), Cache coherence protocols, Reduced energy consumption, Fault tolerance in CMPs, Hardware transactional memory, Synchronization primitives, Multiprocessor architectures, Cache coherence protocols for SMPs and cc-NUMAs, Parallel programming environments, Performance evaluation

EDUCATION

Sept'98 – Mar'03 Ph.D. Degree in Computer Science
“Improving the Performance and Scalability of
Directory-based Shared Memory Multiprocessors”
Facultad de Informática - Universidad de Murcia
Advisors: José Duato (UPV) and José M. García (UM)
Best Thesis Award (Jan. 2004 – Facultad de Informática – UM)

Sept'96 – Jul'98 M.S., Computer Science
Facultad de Informática - Universidad de Murcia

Sept'93 – Jul'96 B.S., Electrical Engineering
Facultad de Informática - Universidad de Murcia

EXPERIENCE

Oct'99 – Present Universidad de Murcia
Departamento de Ingeniería y Tecnología de Computadores
Position: Associate Professor
Courses:

- Introduction to Computer Organization
- Computer Architecture
- Advanced Computer Architecture
- Embedded and Real-Time Systems

Jul 1, 02 – Aug 30, 02 Summer Internship at IBM T.J. Watson Research Center
Yorktown Heights (NY)
BlueGene System Development Dept
Verification of the BlueGene/L compute chip

PUBLICATIONS

JOURNALS

- José L. Abellán, Juan Fernández and Manuel E. Acacio. “Efficient Hardware Barrier Synchronization in Many-Core CMPs”. Accepted in IEEE Transactions on Parallel and Distributed Systems, 2012.
- Rubén Titos-Gil, Manuel E. Acacio, José M. García, Tim Harris, Adrián Cristal, Osman Unsal, Ibrahim Hur and Mateo Valero. “Hardware Transactional Memory with Software-Defined Conflicts”. Accepted in ACM Transactions on Architecture and Code Optimization, 2012.
- Alberto Ros, Blas Cuesta, Ricardo Fernández, María E. Gómez, Manuel E. Acacio, Antonio Robles, José M. García and José Duato. “Extending Magny-Cours Cache Coherence”. Accepted in IEEE Transactions on Computers, 2011.
- Alberto Ros, Manuel E. Acacio and José M. García. “A Direct Coherence Protocol for Many-Core Chip Multiprocessors”. IEEE Transactions on Parallel and Distributed Systems, Vol. 21, No. 12, December 2010.
- Antonio Flores, Juan L. Aragón and Manuel E. Acacio. “Exploiting Address Compression and Heterogeneous Interconnects for Efficient Message Management in Tiled CMPs”. Euromicro Journal of Systems Architecture (JSA), Vol. 56, Issue 9, pp. 429-441, September 2010.
- Ricardo Fernández-Pascual, José M. García, Manuel E. Acacio and José Duato. “Dealing with Transient Faults in the Interconnection Network of CMPs at the Cache Coherence Level”. IEEE Transactions on Parallel and Distributed Systems, Vol. 21, No. 8, August 2010.
- José L. Abellán, Juan Fernández and Manuel E. Acacio. “Characterizing the Basic Synchronization and Communication Operations in Dual Cell-based Blades through CellStats”. Journal of Supercomputing, Vol. 53, No. 2, August 2010.
- Alberto Ros, Manuel E. Acacio and José M. García. “A Scalable Organization for Distributed Directories”. Euromicro Journal of Systems Architecture (JSA), Vol. 56, Issue 2-3, pp. 77-87, February 2010.
- Antonio Flores, Juan L. Aragón and Manuel E. Acacio. “Heterogeneous Interconnects for Energy-Efficient Message Management in CMPs”. IEEE Transactions on Computers, Vol. 59, Issue 1, January 2010.
- Alberto Ros, Ricardo Fernández, Manuel E. Acacio and José M. García. “Two Proposals for the Inclusion of Directory Information in the Last-Level Private Caches of Glueless Shared-Memory Multiprocessors”. Journal of Parallel Distributed Computing, Vol. 68, No. 11, pp. 1413-1424, November 2008.
- Antonio Flores, Juan L. Aragón and Manuel E. Acacio. “An Energy Consumption Characterization of On-Chip Interconnection Networks for Tiled CMP Architectures”. The Journal of Supercomputing, Vol. 45, Issue 3, pp. 341-364, September 2008.
- Ricardo Fernández-Pascual, José M. García, Manuel E. Acacio and José Duato. “Extending the TokenCMP Cache Coherence Protocol for Low Overhead Fault Tolerance in CMP Architectures”. IEEE Transactions on Parallel and Distributed Systems, Vol. 19, No. 8, August 2008.
- Gregorio Bernabé, Ricardo Fernández, José M. García, Manuel E. Acacio and José González. “An Efficient Implementation of a 3D Wavelet Transform Based Encoder on Hyper-Threading Technology”. Parallel Computing Vol. 33, No. 1, pp. 54-72, February 2007.

- Francisco J. Villa, Manuel E. Acacio and José M. García. "Toward Energy-Efficient High-Performance Organizations of the Memory Hierarchy in Chip-Multiprocessor Architectures". *Journal of Computer Science & Technology*, Vol. 6, No. 1, pp. 1-7, April 2006 (*Invited paper*).
- Francisco J. Villa, Manuel E. Acacio and José M. García. "Evaluating IA-32 Web Servers through Simics: A Practical Experience". *Euromicro Journal of Systems Architecture (JSA)* 51, Elsevier, January 2005.
- Manuel E. Acacio, José González, José M. García and José Duato. "A Two-level Directory Architecture for Highly Scalable cc-NUMA Multiprocessors". *IEEE Transactions on Parallel and Distributed Systems*, Vol. 16, No. 1, pp. 67-79, January 2005.
- Manuel E. Acacio, José González, José M. García and José Duato. "An Architecture for High-Performance Scalable Shared-Memory Multiprocessors Exploiting On-chip Integration". *IEEE Transactions on Parallel and Distributed Systems*, Vol. 15, No. 8, pp. 755-768, August 2004.
- Manuel E. Acacio and José M. García. "Techniques for Improving the Performance and Scalability of Directory-based Shared-Memory Multiprocessors: A Survey". *Journal of Computer Science & Technology*, Vol. 3, No. 2, pp. 1-8, October 2003 (*Invited paper*).
- M. E. Acacio, O. Cánovas, J. M. García, P. E. López de Teruel. "MPI-Delphi: An MPI Implementation for Visual Programming Environments and Heterogeneous Computing". *Journal of Future Generation Computer System*, 18 (2002), pp. 317-333, Elsevier Science Publishers, North-Holland, 2002.

CONFERENCES

- José L. Abellán, Juan Fernández, Daniele Bortolotti, Manuel E. Acacio, Andrea Marongiu, Davide Bertozzi and Luca Benini. "Design of a Collective Communication Infrastructure for Barrier Synchronization in Cluster-Based Nanoscale MPSoCs". *Proc. of DATE 2012*, March 2012.
- Anurag Negi, Rubén Titos-Gil, Manuel E. Acacio, José M. García and Per Stenstrom. " π -TM: Pessimistic Invalidation for Scalable Lazy Hardware Transactional Memory". *Proc. of the 18th Int'l Symposium on High Performance Computer Architecture (HPCA-2012)*, February 2012.
- Epifanio Gaona, Rubén Titos-Gil, Juan Fernández and Manuel E. Acacio. "Dynamic Serialization: Improving Energy Consumption in Eager-Eager Hardware Transactional Memory Systems". *Proc. of the 20th Euromicro Conference on Parallel, Distributed and Network-Based Processing (PDP-2012)*, February 2012.
- Rubén Titos-Gil, Manuel E. Acacio, José M. García, Tim Harris, Adrián Cristal, Osman Unsal, Ibrahim Hur and Mateo Valero. "Hardware Transactional Memory with Software-Defined Conflicts". In *7th Int'l Conference on High-Performance and Embedded Architectures and Compilers (HiPEAC 2012)*, January 2012.
- Anurag Negi, Rubén Titos-Gil, Manuel E. Acacio, José M. García and Per Stenstrom. "Improving Commit Scalability in Lazy Hardware Transactional Memory". *Proc. of the 4th Swedish Workshop on Multicore Computing (MCC-2011)*, November 2011.
- Anurag Negi, Rubén Titos-Gil, Manuel E. Acacio, José M. García and Per Stenstrom. "Eager Meets Lazy: The Impact of Write-Buffering on Hardware Transactional Memory". *Proc. of the 40th Int'l Conference on Parallel Processing (ICPP-2011)*, September 2011.
- Rubén Titos-Gil, Anurag Negi, Manuel E. Acacio, José M. García and Per Stenstrom. "ZEBRA: A Data-Centric, Hybrid-Policy Hardware Transactional Memory Design". *Proc. of the 25th Int'l Conference on Supercomputing (ICS-2011)*, May 2011.
- Anurag Negi, Rubén Titos-Gil, Manuel E. Acacio, José M. García and Per Stenstrom. "The Impact of Non-coherent Buffers on Lazy Hardware Transactional Memory Systems". *Proc. of the 13th*

Workshop on Advances on Parallel and Distributed Processing Symposium (APDCM 2011), in conjunction with IPDPS 2011, May 2011.

- José L. Abellán, Juan Fernández and Manuel E. Acacio. "GLocks: Efficient Support for Highly-Contented Locks in Many-Core CMPs". Proc. of the 25th IEEE Int'l Parallel and Distributed Processing Symposium (IPDPS 2011), May 2011 (Best Paper in the Architecture Track).
- Alberto Ros, Blas Cuesta, Ricardo Fernández, María E. Gómez, Manuel E. Acacio, Antonio Robles, José M. García and José Duato. "EMC2: Extending Magny-Cours Coherence for Large-Scale Servers". Proc. of 17th Annual IEEE International Conference on High Performance Computing (HiPC 2010), December 2010.
- Epifanio Gaona, Rubén Titos, Juan Fernández and Manuel E. Acacio. "Characterizing Energy Consumption in Hardware Transactional Memory Systems". Proc. of the 22nd Int'l Symposium on Computer Architecture and High Performance Computing (SBAC-PAD 2010), October 2010.
- José L. Abellán, Juan Fernández and Manuel E. Acacio. "A G-line-based Network for Fast and Efficient Barrier Synchronization in Many-Core CMPs". Proc. of the 39th Int'l Conference on Parallel Processing (ICPP 2010), September 2010.
- Alberto Ros and Manuel E. Acacio. "Low-Overhead Organizations for the Directory in Future Many-Core CMPs". Proc. of the 4th Workshop on Highly Parallel Processing on a Chip (HPPC 2010), September 2010.
- José L. Abellán, Juan Fernández and Manuel E. Acacio. "Efficient and Scalable Barrier Synchronization for Many-Core CMPs". Proc. of the ACM Int'l Conference on Computing Frontiers 2010, May 2010.
- Rubén Titos-Gil, Manuel E. Acacio, José M. García, Tim Harris, Adrián Cristal, Osman Unsal, Ibrahim Hur and Mateo Valero. "Hardware Transactional Memory with Software-Defined Conflicts". 5th ACM SIGPLAN Workshop on Transactional Computing (TRANSACT 2010), April 2010.
- Antonio Flores, Juan L. Aragón and Manuel E. Acacio. "Energy-Efficient Hardware Prefetching for CMPs using Heterogeneous Interconnects". Proc. of the 18th Euromicro Conference on Parallel, Distributed and Network-Based Processing (PDP-2010), February 2010.
- José L. Abellán, Juan Fernández and Manuel E. Acacio. "A Novel Hardware-based Barrier Synchronization for Many-Core CMPs". 4th Workshop on Interconnection Network Architectures: On-Chip, Multi-Chip (INA-OCMC 2010), January 2010.
- Alberto Ros, Marcelo Cintra, Manuel E. Acacio y José M. García. "Distance-Aware Round-Robin Mapping for Large NUCA Caches". Proc. of the 16th Annual IEEE International Conference on High Performance Computing (HiPC 2009), December 2009.
- Alberto Ros, Manuel E. Acacio y José M. García. "Dealing with Traffic-Area Trade-Off in Cache Coherence Protocols for Many-Core CMPs". Proc. of the 8th International Conference on Advanced Parallel Processing Technologies (APPT 2009), August 2009.
- Epifanio Gaona, Juan Fernández and Manuel E. Acacio. "Fast and Efficient Synchronization and Communication Collective Primitives for Dual Cell-based Blades". Proc. of Euro-Par 2009, August 2009.
- Rubén Titos, Manuel E. Acacio and José M. García. "Speculation-Based Conflict Resolution in Hardware Transactional Memory". Proc. of the 23rd IEEE Int'l Parallel and Distributed Processing Symposium (IPDPS 2009), May 2009.
- Joaquín Franco, Gregorio Bernabé, Manuel E. Acacio and Juan Fernández. "A Parallel Implementation of the 2D Wavelet Transform Using CUDA". Proc. of the 17th Euromicro Conference on Parallel, Distributed and Network-Based Processing (PDP-09), February 2009.

- Ricardo Fernández-Pascual, José M. García, Manuel E. Acacio and José Duato. “Fault-Tolerant Cache Coherence Protocols for CMPs: Evaluation and Trade-offs”. Proc. of the 15th Annual IEEE International Conference on High Performance Computing (HiPC 2008), December 2008.
- Rubén Titos, Manuel E. Acacio and José M. García. “Directory-Based Conflict Detection in Hardware Transactional Memory”. Proc. of the 15th Annual IEEE International Conference on High Performance Computing (HiPC 2008), December 2008.
- Antonio Flores, Manuel E. Acacio and Juan L. Aragón. “Address Compression and Heterogeneous Interconnects for Energy-Efficient High-Performance Tiled CMPs”. Proc. of the 37th International Conference on Parallel Processing (ICPP-08), September 2008.
- Alberto Ros, Manuel E. Acacio y José M. García. “Scalable Directory Organization for Tiled CMP Architectures”. Proc. of the Int’l Conference on Computer Design (CDES), July 2008.
- José L. Abellán, Juan Fernández and Manuel E. Acacio. “Characterizing the Basic Synchronization and Communication Operations in Dual Cell-Based Blades”. Proc. of the Int’l Conference on Computational Science (ICCS 2008), June 2008.
- Ricardo Fernández-Pascual, José M. García, Manuel E. Acacio and José Duato. “A Fault-Tolerant Directory-Based Cache Coherence Protocol for CMP Architectures”. Proc. of the 38th Annual IEEE/IFIP International Conference on Dependable Systems and Networks (DSN-DCCS), June 2008.
- Alberto Ros, Manuel E. Acacio and José M. García. “DiCo-CMP: Efficient Cache Coherency in Tiled CMP Architectures”. Proc. of the 22nd IEEE International Parallel and Distributed Processing Symposium (IPDPS 2008), April 2008.
- José L. Abellán, Juan Fernández and Manuel E. Acacio. “CellStats: a Tool to Evaluate the Basic Synchronization and Communication Operations of the Cell BE”. Proc. of the 16th Euromicro Conference on Parallel, Distributed and Network-Based Processing (PDP-08), February 2008.
- Rubén Titos, Manuel E. Acacio and José M. García. “A Characterization of Conflicts in Log-Based Transactional Memory (LogTM)”. Proc. of the 16th Euromicro Conference on Parallel, Distributed and Network-Based Processing (PDP-08), February 2008.
- Alberto Ros, Manuel E. Acacio and José M. García. “Direct Coherence: Bringing Together Performance and Scalability in Shared-Memory Multiprocessors”. Proc. of the 14th Int’l Conference on High Performance Computing (HiPC 2007), December 2007.
- Antonio Flores, Juan L. Aragón and Manuel E. Acacio. “Efficient Message Management in Tiled CMP Architectures using a Heterogeneous Interconnection Network”. Proc. of the 14th Int’l Conference on High Performance Computing (HiPC 2007), December 2007.
- Antonio Flores, Juan L. Aragón and Manuel E. Acacio. “Sim-PowerCMP: A Detailed Simulator for Energy Consumption Analysis in Future Embedded CMP Architectures”. Proc. of the 4th IEEE Int’l Symposium on Embedded Computing (SEC-07), May 2007.
- Ricardo Fernández-Pascual, José M. García, Manuel E. Acacio and José Duato. “A Low Overhead Fault Tolerant Coherence Protocol for CMP Architectures”. Proc. of the 13th Int’l Symposium on High Performance Computer Architecture (HPCA-13), February 2007.
- Francisco J. Villa, Manuel E. Acacio and José M. García. “On the Evaluation of Dense Chip-Multiprocessor Architectures”. Proc. of the 2006 Int’l Conference on Embedded Computer Systems: Architectures, MOdeling, and Simulation (IC-SAMOS VI), July 2006.
- Ricardo Fernández-Pascual, José M. García and Manuel E. Acacio. “Validating a Token Coherence Protocol for Scientific Workloads”. Proc. of the 5th Annual Workshop on Duplicating, Deconstructing, and Debunking (WDDD 2006), held in conjunction with ISCA-33, June 2006.

- Alberto Ros, Manuel E. Acacio and José M. García. “An Efficient Cache Design for Scalable Glueless Shared-Memory Multiprocessors”. Proc. of the 2006 ACM Int’l Conference on Computing Frontiers, May 2006.
- Francisco J. Villa, Manuel E. Acacio and José M. García. “Memory Subsystem Characterization in a 16-core Snoop-Based Chip-Multiprocessor Architecture”. Proc. of the 2005 International Conference on High Performance Computing and Communications (HPCC), LNCS 3726, September 2005.
- Alberto Ros, Manuel E. Acacio and José M. García. “A Novel Lightweight Directory Architecture for Scalable Shared-Memory Multiprocessors”. Proc. of the Euro-Par 2005 Conference, LNCS 3648, September 2005.
- Ricardo Fernández, Gregorio Bernabé, José M. García and Manuel E. Acacio. “Optimizing a 3D-FWT Video Encoder for SMPs and HyperThreading Architectures”. Proc. of the 13th Euromicro Conference on Parallel, Distributed and Network-based Processing (PDP-05), February 2005.
- Francisco J. Villa, Manuel E. Acacio and José M. García. “On the Evaluation of x86 Web Servers Using Simics: Limitations and Trade-Offs”. Proc. of the 4th International Conference on Computational Science, LNCS 3036, pp. 541-544, Krakow (Poland), June 2004.
- Manuel E. Acacio, José González, José M. García and José Duato. “Owner Prediction for Accelerating Cache-to-Cache Transfer Misses in cc-NUMA Multiprocessors”. Proc. of the SC2002 High Performance Networking and Computing, November 2002.
- Manuel E. Acacio, José González José M. García and José Duato. “The Use of Prediction for Accelerating Upgrade Misses in cc-NUMA Multiprocessors”. Proc. of the 2002 International Conference on Parallel Architectures and Compilation Techniques (PACT 2002), September 2002.
- Manuel E. Acacio, José González José M. García and José Duato. “A Novel Approach to Reduce L2 Miss Latency in Shared-Memory Multiprocessors”. Proc. of the 14th Int’l Parallel and Distributed Processing Symposium (IPDPS 2002), April 2002.
- Manuel E. Acacio, José González José M. García and José Duato. “Reducing the Latency of L2 Misses in Shared-Memory Multiprocessors through On-Chip Directory Integration”. Proc. of the 10th Euromicro Workshop on Parallel, Distributed and Network-based Processing (PDP-02), January 2002.
- Manuel E. Acacio, José González José M. García and José Duato. “A New Scalable Directory Architecture for Large-Scale Multiprocessors”. Proc. of the 7th Int’l Symposium on High Performance Computer Architecture (HPCA-7), January 2001.
- M. Acacio, J.M. García, P.E. López de Teruel and O. Cánovas. "The MPI-Delphi Interface: A Visual Programming Environment for Clusters of Workstations". Proc. of the Int’l Conference on Parallel and Distributed Processing Techniques and Applications (PDPTA'99), CSREA Press, June 1999.
- P.E. López de Teruel, J.M. García, M.E. Acacio and O. Cánovas. "P-EDR: An Algorithm for Parallel Implementation of Parzen Density Estimation from Uncertain Observations". Proc. of the 11th Int’l Parallel and Distributed Processing Symposium (IPDPS 1999), April 1999.
- M. Acacio, O. Cánovas, J.M. García and P.E. López de Teruel. "An Evaluation of Parallel Computing in PC Clusters". Proc. of the 4th Int’l ACPC Conference on Parallel Computing (ACPC'99), Lecture Notes in Computer Science 1557, February 1999.

BOOK CHAPTERS

- Alberto Ros, Manuel E. Acacio y José M. García. "Cache Coherence Protocols for Many-Core CMPs". Parallel and Distributed Computing, In-Tech, January 2010. ISBN: 978-953-307-057-5.

PROFESSIONAL ACTIVITIES

- Reviewer for: ISCA-2001, SPAA-2001, CAC-2002 (Workshop held in conjunction with the IPDPS-2002), SC-2002, ICS-2003, PACT-2003, ISHPC-03, AC-2004, IPDPS 2004, SBACPAD-2004, HPCA-2005, CGO-2005, IPDPS-2005, AC-2005, ICPP-2005, HPCA-2006, IPDPS-2006, AC-2006, ISCA 2006, ICPADS-2006, AC-2007, Europar 2007, ICS 2007, AC-2008, PACT-2008, HOTI-2008, ISCA-2010, ISLPED 2010, HPCA-2010, Journal of Parallel and Distributed Computing, IEE Proceedings Computers and Digital Techniques, IEEE Transactions on Parallel and Distributed Systems, International Journal of Computers and Applications, IEEE Transactions on VLSI, IEEE Computer Architecture Letters
 - Committee Member of the IASDIS AC-2004, AC-2005, AC-2006, AC-2007, AC-2008, ICPP-2005, ICPADS-2006, IPM/ESA/RFID 2007, IPDPS 2009, ICES 2009, EmbeddedCom 2009, ICES 2010
 - Associate Editor of IEEE Transactions on Parallel and Distributed Systems
 - Member of the HiPEAC European Network of Excellence (www.hipeac.org)
 - Participant in the Euro-TM COST Action (www.eurotm.org)
-